WHAT IS CLAIMED IS:

1. An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and

a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the first base layer a channel electrically connecting between the source layer and the second base layer,

wherein the injection efficiency of hole current from said drain layer is 0.27 in maximum.

2. The insulated gate semiconductor device according to claim 1, wherein thickness of the first base layer is 70 μm in maximum.

3. An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and

a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the first base layer a channel electrically connecting between the source layer and the second base layer,

wherein the voltage transiently applied to said device is larger than the static breakdown voltage between the source

and the drain when a rated current is turned off under a condition, in which condition an inductance load is from 1 μH to 1mH and said device is connected said inductance load without using a protective circuit, and wherein thickness of the first base layer is 70 μm in maximum.

4. An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and

a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the first base layer a channel electrically connecting the source layer and the second base layer,

wherein the injection efficiency of hole current from the drain layer is less than 9/19.

5. The insulated gate semiconductor device according to claim 4, wherein thickness of the first base layer is 70 μm in maximum.

6. An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the first conduction type formed on a first surface of the first base layer and having a thickness not larger than 0.5 μm; and

a gate electrode insulated from the source layer, the

first base layer and the second base layer and forming in the first base layer a channel electrically connecting the source layer and the second base layer,

wherein the voltage transiently applied to said device is larger than the static breakdown voltage between the source and the drain when a rated current is turned off under a condition, in which condition an inductance load is from 1 μH to 1mH and said device is connected said inductance load without using a protective circuit, and wherein thickness of the first base layer is 70 μm in maximum.

7. The insulated gate semiconductor device according to claim 1 further comprising:

a buffer layer of the first conduction type which is lower in resistance value than the first base layer and which is located between the first base layer and the drain layer.

8. The insulated gate semiconductor device according to claim 3 further comprising:

a buffer layer of the first conduction type which is lower in resistance value than the base layer of the first base layer and which is located between the first base layer and the drain layer.

9. The insulated gate semiconductor device according to claim 4 further comprising:

a buffer layer of the first conduction type which is lower in resistance value than the base layer of the first base layer and which is located between the first base layer and the drain layer.

10. The insulated gate semiconductor device according to claim 6 further comprising:

a buffer layer of the first conduction type which is lower in resistance value than the base layer of the first base layer and which is located between the first base layer and the drain layer.

11. The insulated gate semiconductor device according to claim 7, wherein the buffer layer of the first conduction type includes a plurality of layers different in resistance value from each other.

12. The insulated gate semiconductor device according to claim 8, wherein the buffer layer of the first conduction type includes a plurality of layers different in resistance value from each other.

13. The insulated gate semiconductor device according to claim 9, wherein the buffer layer of the first conduction type includes a plurality of layers different in resistance value from each other.

14. The insulated gate semiconductor device according to claim 10, wherein the buffer layer of the first conduction type includes a plurality of layers different in resistance value from each other.

15. The insulated gate semiconductor device according to claim 7, wherein the buffer layer of the first conduction type includes two stepwise layers having a low concentration and a high concentration respectively.

16. The insulated gate semiconductor device according to claim 8, wherein the buffer layer of the first conduction type includes two stepwise layers having a low concentration and a high concentration respectively.

17. The insulated gate semiconductor device according to claim 9, wherein the buffer layer of the first conduction type includes two stepwise layers having a low concentration and a high concentration respectively.

18. The insulated gate semiconductor device according

to claim 10, wherein the buffer layer of the first conduction type includes two stepwise layers having a low concentration and a high concentration respectively.

19. An insulated gate semiconductor device comprising:

a first base layer of a first conduction type;

a second base layer of a second conduction type formed on a first surface of the first base layer;

a source layer of the first conduction type selectively formed in a surface region of the second base layer;

a drain layer of the second conduction type formed on a second surface of the first base layer opposite from said first surface; and

a gate electrode insulated from the source layer, the first base layer and the second base layer and forming in the first base layer a channel electrically connecting the source layer and the second base layer,

wherein the total impurity dose of the drain layer is $5 \times 10^{13} cm^{-2}$ in maximum.

20. The insulated gate semiconductor device according to claim 19, wherein thickness of the drain layer is 5 μm in maximum.